Pulsed Class-G RF Amplifier System

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First off we would like to thank Professor Vladimir Prodanov, for allowing us to work on this project, also for helping us at every step along the way while keeping us on task. We would also like to thank NXP for donating the BLF6G27-10 power transistor demo board. Also TI's donation, specifically the HSP Data Converters group and the WBI Radio Products group, of the TSW3100 and the TSW30H84 signal generator boards was vital to the testing of our design. Without these donations we would not have been able to complete this project. We would also like to thank Cal Poly for letting us use their equipment, including the spectrum analyzer, frequency synthesizer, and the oscilloscope.

ABSTRACT

In the field of RF power amplifiers, RF engineers confront difficult decisions based on design tradeoffs. Most importantly, tradeoff between linearity and efficiency leads the list of issues RF amplifier designers face. Class AB amplifiers are currently the most commonly used amplifier architectures used in RF systems due to their relative balance of linearity and efficiency allowing designers to implement additional linearization and efficiency-boosting techniques. Furthermore, this design project seeks to improve power efficiency of a Class AB RF power amplifier architecture while maintaining device linearity. In today's wireless communication systems, RF power amplifiers are required to amplify signals with ever more large peak-to-average power ratios (PAPR or just PAR). Therefore, the project focuses on a power efficiency boosting technique to accommodate these large PAR signals associated with OFDM and LTE (Long Term Evolution) modulation types.

INTRODUCTION

RF power amplifier design focuses on the tradeoff between linearity and efficiency, both of which are extremely important to robust design. Couple the previous statement with the increasingly high PAPR (peak-to-average power ratio) of current transmitted RF communication signals and the task of RF amplifier design becomes proportionally more difficult [9].

Both efficiency and linearity of an amplifier are dependent on the level of power supplied to the device. With input signals with large PAR, choosing a constant supply will compromise one or both of linearity and efficiency. With linearity taking precedent over efficiency, large PAR brings about reduced efficiency of RF power amplifiers [9]. For example, the maximum power efficiency of a class-B PA is 78.5%, but when accounting for a signal having a PAR of 10dB, efficiency drops to 7.85%.[2] As a result, RF engineers seek to employ techniques to adapt to high PAR signals. One of these techniques, known as the class-G/class-H power amplifier, adjusts power supply specs in response to input signal information. Such amplifiers require some form of feed-forward topology.

Typical class-G/H power amplifiers employ class-AB output stages and apply various techniques to adjust power supply specs. Furthermore, the power surge class-G RF power amplifier seeks to implement a new technique to adjust power supply specification to the class-AB amplifier. More specifically, the design doubles the supply voltage when the signal reaches a certain input power. Furthermore, voltage doubling designs can be implemented using capacitors and their capability to store energy provided by the nominal DC supply. With that in mind, statistical analysis is required to determine suitable capacitor size due to the fact that doubling duration depends on the discharging time of the capacitor. Implementing a capacitor-based voltage doubling design also seeks to reduce cost of class-G/H amplifier topologies.

Establishing the Problem: High PAR Signal Analysis:

Many wireless applications today employ orthogonal frequency division multiplexing (OFDM), including DSL broadband internet access and 4G mobile communications. An OFDM signal is made up of many closely spaced complex modulated carriers with guard bands in-between to allow the receiver to distinguish between carriers. Furthermore, an OFDM signal is the combination of complex modulated sinusoidal sub- carriers that are mixed up to a high frequency, giving it a bandwidth that is dependent on the number of sub-carriers and their spacing [9].

The OFDM time waveform is the total of the magnitude and phase of all the subcarrier sine waves. The points in figure 1 to the right represent the location of each carrier of an OFDM signal. When adding multiple sinusoidal sub-carriers together, peaking occurs when the sub-carriers are in phase with each other. Therefore, the maximum possible peak occurs when every sub-carrier is at their individual peak value and are all in phase, resulting in a voltage equal to all their values added up. Although rare, peaking occurs and must be taken into account in the design of nonlinear RF components.

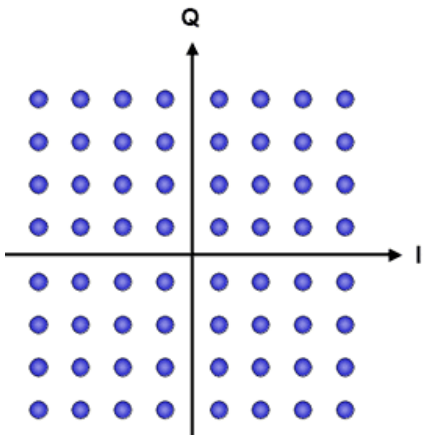

Figure 1: Constellation of OFDM

The peak to average power ration is defined as

$$\text{papr} = \frac{\max\left[x(t)x^*(t)\right]}{E[x(t)x^*(t)]}$$. Where the max is the maximum seen value and E is the expected, average value [9]. The transmitted signal, (sum of all complex sinusoids) can be written as

$x(t) = \sum_{0}^{K-1} a_K e^{\frac{j2\pi kt}{T}}$. Where K is the number of subcarriers, T is the distance between them, and a_K is the weight of each individual subcarrier. I a_K is assumed to be 1 for all subcarriers the maximum value is K^2. The expected power value of an OFDM signal is equal to K. Therefore

$PAPR = \frac{K^2}{K} = K$. A PAPR of this value will never occur because this assumes all the subcarriers are equally weighted ($a_K = 1$). It also assumes that the highest value of the signal occurs when all subcarriers are in phase, which is very unlikely to occur. What can be expected from this though, is that the more subcarriers in an OFDM signal the higher its PAPR value will be [9].

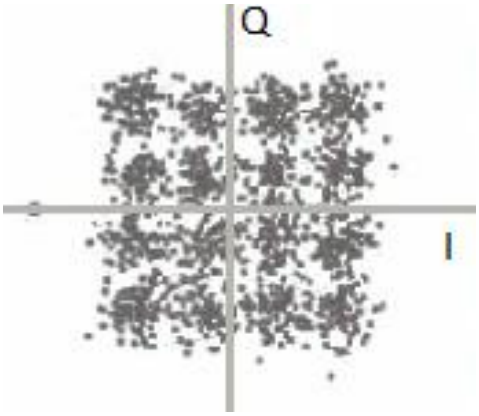

Figure 2: Constellation of LTE

The only difference between a long-term evolution (LTE) signal and an OFDM signal is the location of each point in its constellation diagram, shown in figure 2, is randomized. This is to reduce the likelihood of all the subcarriers aligning in phase and adding up to a high peak value.

REQUIREMENTS AND SPECIFICATIONS

In order to set forth on the system design, the capabilities of the product must be known. Laying down a foundation for what the device should accomplish allows the designers to understand what goals need to be met. To do so, the following table, outlines the marketing requirements and engineering specifications of the power surge class-G RF power amplifier system.

TABLE I

POWER AMPLIFIER MODULE REQUIREMENTS AND SPECIFICATIONS [3]-[4]

Marketing Requirements	**Engineering Specifications**	**Justification**
4	Max Frequency: Frequency range suitable for OFDM, WiMax, 4G signal.	PA provides gain for this frequency range which is used for cellular communications.
1	Output power (P_{out}) ~= 40dBm (10W)	For medium range base station transmitters, the upper limit of rated output power is 40dBm. Switched supply must maintain output power characteristics of class-AB power amplifier.
3, 5	Adjacent channel leakage ratio : 5MHz above highest carrier and below lowest carrier, 45 dB; 10MHz above highest carrier and below lowest carrier, 50dB.	Regulating the power delivered to out of band emissions improves linearity and efficiency. Switching the transistor drain supply must not compromise distortion caused by rail clipping
2	Power of spurious emissions shall not	Spurious emissions cause in band

	exceed -13dB	distortion and therefore limiting them reduces in-band distortion and maintains the integrity of the signal information.
6	Input signal: OFDM, WiMax, 4G. Needs to have >9dB PAPR	Power amplifier should be able to amplify the specified input signals (mod type) linearly.
1	Gain : 19 dB @ +/- 0.5 dB flatness.	Gain of power amplifier should be sufficient enough to increase input power to specified output power. Furthermore, switched power supply must maintain this gain.
1, 3	DC Power Supply: Switched from 14V to 28V	Active device must be DC biased in order to define region of operation (of transistor) and necessary gain. DC supply must be chosen to maximize added power and reduce DC power.
3	Power-added-efficiency: > 50%	Power added efficiency is a measure of power amplifier efficiency and maximizing the figure requires the amplifier to get the most power out of the dc power supplied.

Marketing Requirements

1. Deliver sufficient power to amplifier
2. Limit in-band distortion
3. Efficient
4. Defined frequency range (bandwidth) of operation

5. Reduce out-of-band emissions

6. Amplify low power, high PAR RF input

Functional Decomposition

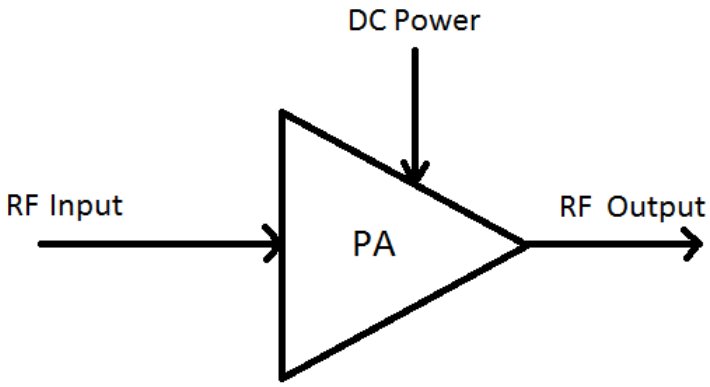

Figure 3: Level 0 Class G RF Power Amplifier Block Diagram

Table II
LEVEL 0 CLASS G RF POWER AMPLIFIER FUNCTIONALITY

Module	RF Power Amplifier (PA)
Inputs	RF input signal: modulation type - OFDM, WiMax, 4G, LTE DC Power Supply: 20-30V
Output	RF output signal: <40dBm
Functionality	Amplify an RF input signal with gain of 20-25 dB over specified frequency band to a 50 Ω load.

The power surge class-G RF amplifier has two inputs and one output, as shown in figure 3. The module requires an RF signal input and DC power input in order to produce an amplified RF output signal. The module converts the DC power input into RF power that adds with the low power RF input signal to increase RF power out. Specifically, the module accepts input RF signals with large PAR characteristic of current modulation types (WiMax, OFDM, 4G, LTE, etc). In order to limit problems related to high power signals, the output power of the module should remain below 10W (40dBm).

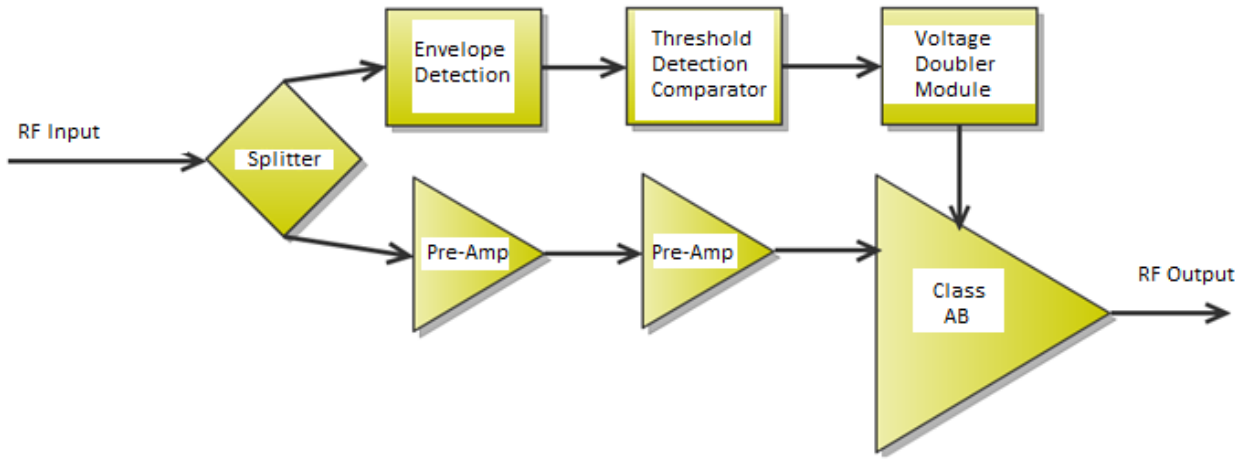

Figure 4: Level 1 Class G RF Power Amplifier Block Diagram

As stated earlier, typical class-G power amplifiers include class-AB biased amplifiers accompanied by various techniques to modulate the DC supply input signal based on RF input signal information. Furthermore, the power surge class-G RF amplifier uses a form of feed-forward to modulate the DC supply input signal. The layout of this design is depicted in figure 4, above. The system employs an envelope detector to obtain information about the instantaneous input power of the RF input signal. Based on this information, the DC supply voltage doubles when the input RF power exceeds the point where the output signal would exceed un-switched supply rail (half supply).

DESIGN

The following design focuses around the NXP 2.5-2.7 GHz class-AB power amplifier evaluation module, which is detailed further in the test plans section. Therefore, design of the pulsed class-G power amplifier consists of design and integration of the feed-forward path from RF input to class-AB amplifier drain supply [2]. Furthermore, an envelope detection device must be chosen to provide an output range compatible with a properly biased, fast switching comparator, whose output range must drive the buffer controlling the supply switching doubler. These three functional blocks of the feed-forward path are now discussed.

Envelope Detection:

Requirements: The envelope detector is to take in a large PAR signal and output a signal proportional to the envelope of the input waveform.

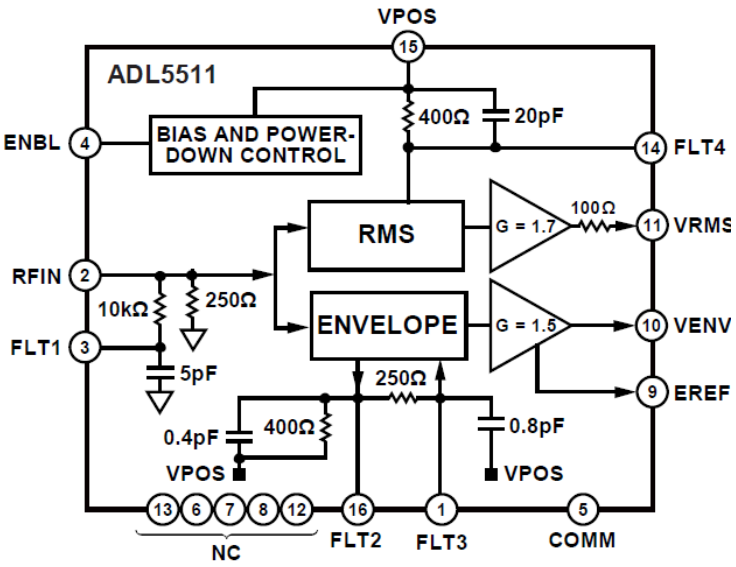

Figure 5: Equivalent circuit of envelope detector and evaluation board [1]

The envelope detector chosen, Analog Devices' ADL5511 [1], figure 5, accepts a signal from DC to 6GHz and outputs a voltage proportional to the instantaneous input power. This envelope output contains enough information concerning the signal being amplified by the class-AB amplifier to drive the threshold detector. In order to integrate the envelope detector into the system, the transfer characteristics must first be determined through testing of the module by itself. The following (figure 6) external circuitry needs to be added to allow for optimal operation above 1GHz.

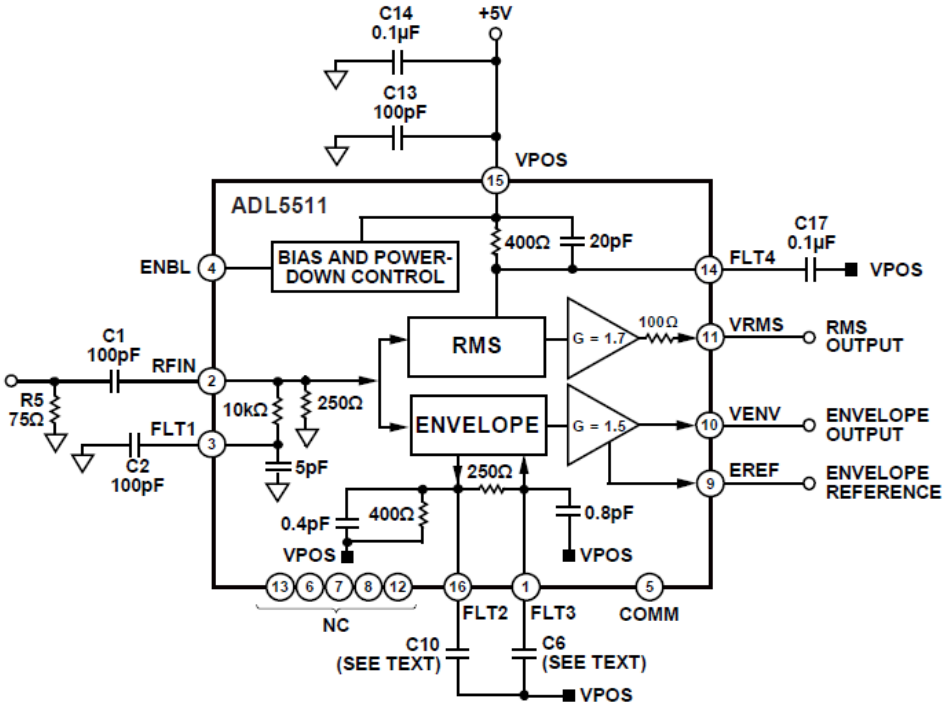

Figure 6: Envelope Detector Bias Circuitry [1]

To test the envelope voltage output range, apply a constant amplitude sinusoid signal at the RF input and record the voltage seen on the output. The actual testing consists of applying a 2.6GHz CW signal with input power ranging from -10dBm to 13dBm. The results of the test are shown in figure 7 below and tabulated values are located in Appendix E.

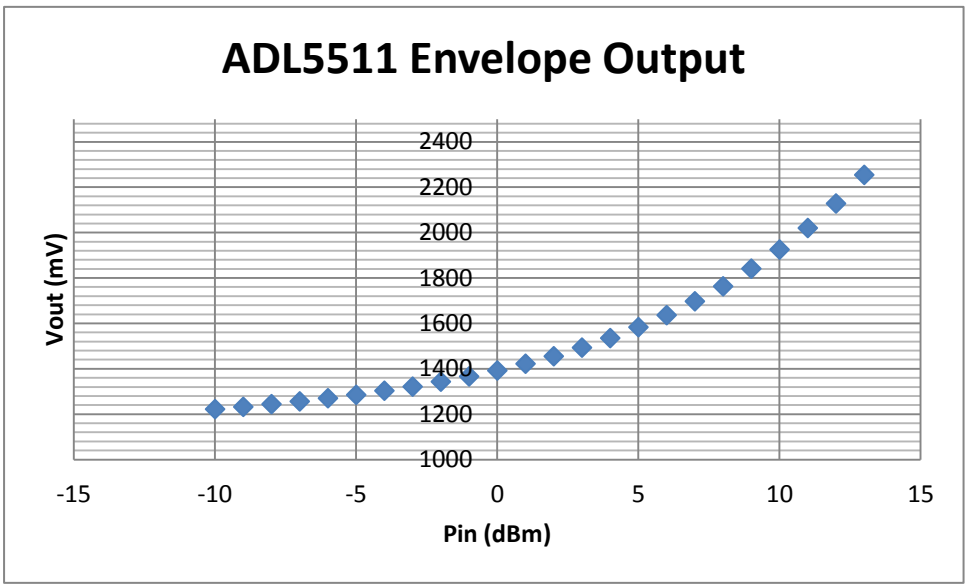

Figure 7: Envelope Voltage versus input power of envelope detector

From the test results above, the comparator can be designed around the output characteristics of the envelope detection.

Hysteretic Comparator:

Requirements: The comparator design should be capable of receiving the range of voltages being supplied by the envelope detection block and output a "low" voltage when this envelope voltage is below a designed threshold and output a "high" voltage when the envelope voltage is above a designed threshold. In order to avoid flickering around a single threshold the comparator needs to be implemented with hysteresis.

The comparator stage implements the Analog Devices ADCMP602 [4]. In theory, comparators simply compare the voltages on its inverting and non-inverting inputs and output logic high, when the non-inverting input is greater than the inverting input, or logic low, when the non-inverting input is less than the inverting input. Figure 8 below, contains the functional circuit diagram of the ADCMP602 comparator.

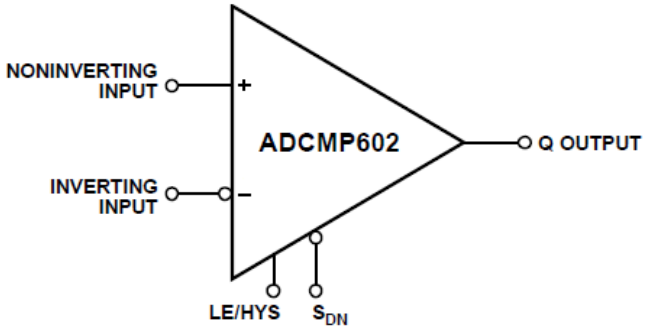

Figure 8: Functional block diagram of voltage comparator [4]

One important characteristic to realize about this specific comparator is that the output voltage swings from rail to rail. Within datasheet specification, a 5V supply connects to the input/output V_{CC} pins of the comparator, therefore the output swings from 0 (GND pin) to 5 volts depending on the comparison of the two inputs. An output voltage swing of 0 to 5 volts needs to drive the buffer gate, which controls the supply switching (voltage doubler) and will be clarified in the next design section [4].

Also, the ADCMP602 comparator has dual front-end design, meaning some of the internal devices are active near the positive rail and others are active near the ground rail. At a predetermined point in the common-mode range, usually half of the positive supply rail, a crossover occurs [4]. At a crossover point the direction of the bias current reverses and the measured offset voltages and currents change. By examining the comparators data sheet [4], the crossover points are at 0.8V and 1.6V. These crossover points need to be avoided when setting the threshold voltage. Therefore, designing the comparator to switch around 1.3 V (with hysteresis) accommodates the output characteristic of the envelope detector and stays away from these crossover points. Acquiring a threshold level of 1.3 V consists of setting the inverting pin on the ADCMP602 to 1.3V by voltage dividing down from the 5V supply rail (shown in Figure 9).

$\frac{R_2}{R_1+R_2}(5V) = 1.3V$ (Choose R1= 10kΩ; solve for R_2) $R_2 = 3.51$ kΩ

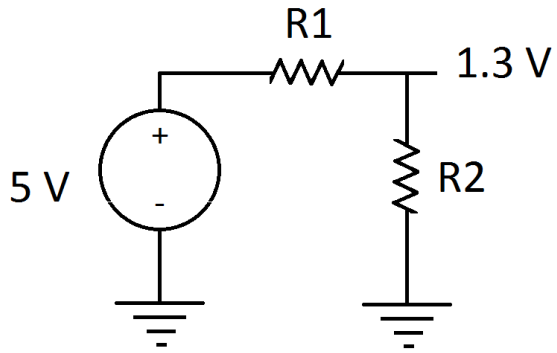

Figure 9: Setting threshold voltage at inverting input of comparator.

Another characteristic that the ADCMP602 provides is adjustable hysteresis by means of a resistor to ground, connected to the (very convenient) hysteresis pin of the chip. As stated earlier, hysteresis prevents the output voltage of the comparator from "flickering" between high and low when the inputs are comparable. Furthermore, hysteresis causes threshold voltage for transitions from low to high to be greater than the threshold voltage for transitions from high to low. Choosing a 160kΩ resistor will provide approximately 50mV of hysteresis (shown in Figure 10, below), which provides enough separation between the two types of transitions.

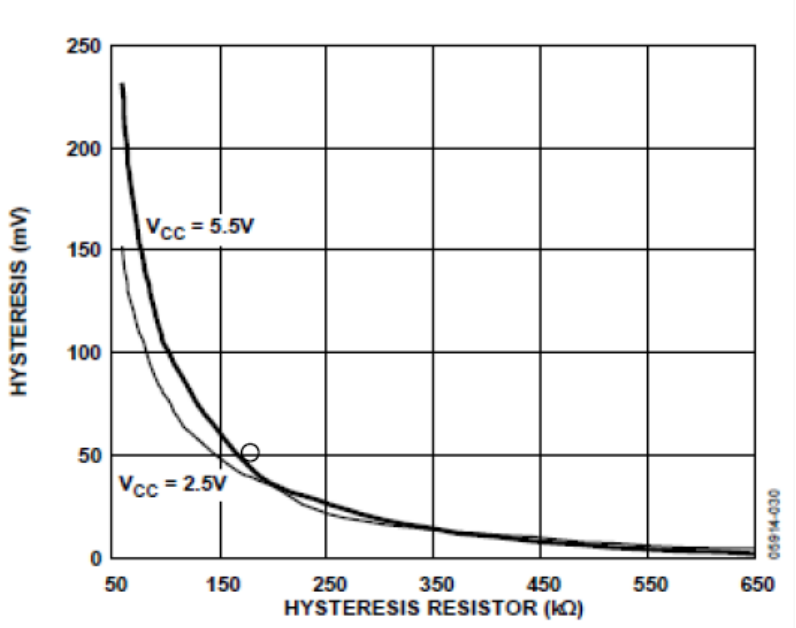

Figure 10: Setting the hysteresis with a resistor for the comparator

By setting the threshold to 1.3V and providing 50mV of hysteresis by connecting a 160kΩ resistor to the hysteresis pin to ground, the plot shown in figure 11, displays the specific input to output voltage transfer characteristic. Output transitions from low to high occur when the non-inverting input exceeds a voltage of 1.325V [4]. Conversely, output transitions from high to low occur when the non-inverting input decreases below a voltage of 1.225V from a voltage greater than 1.225 Again, this characteristic is mostly to prevent noisy "flickering" that would occur due to a single threshold.

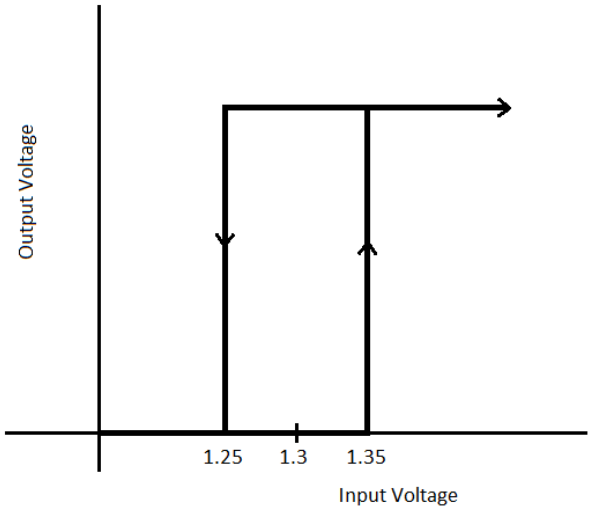

Figure 11: Transfer characteristic for the comparator design

Voltage Doubler:

Requirements: The voltage doubler takes in two inputs, switching control signal and 14V supply, and output either 14V (directly from the input supply) or 28V (the nominal drain voltage for a base station power amplifier).

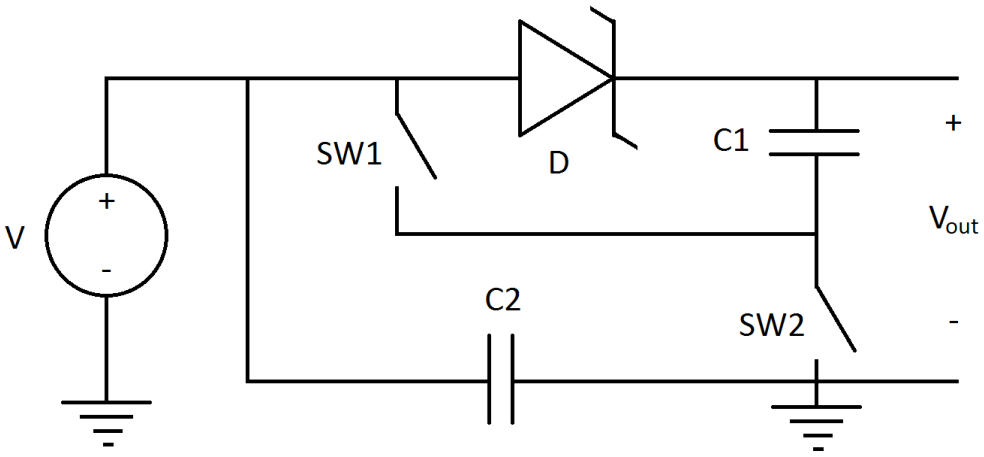

Figure 12: Voltage Doubler Schematic

Figure 12, above, shows the basis of the ideal voltage doubler design. To consider the voltage doubler ideal, the switches need to operate with zero loss when they are shorted (as well as various other ideal characteristics, and the diode needs to have zero voltage drop when forward biased.

To understand the theory of operation of this circuit it is important to note two transient responses based on the state of the ideal switches (SW1 is open when SW2 is shorted, and SW1 is shorted when SW2 is open). Capacitor C1 charges when SW1 is open and SW2 is shorted. Equivalently, the circuit looks like a voltage source in series with a forward biased diode and capacitor C1 (ignore C2). Once fully charged C1 acts like an open circuit and the circuit outputs 14V (half supply). When SW2 opens and consequently SW1 shorts, the equivalent circuit looks like the 14V supply in series with capacitor C1. Since capacitor C1 has 14V potential difference across its plates, the circuit initially outputs 28V but then decays to 14V (capacitor discharges from 14V to 0V).

To accomplish implementing the ideal switches shown above, a buffer gate can be used. When choosing a buffer gate, the device needs to be able to run off a supply of 14V or greater, drive a minimum of 2A (pulsed), and contain transistors with minimal on resistance. Texas Instruments manufactures the UCC27424D dual non-inverting buffer chip, which can run off of a supply of up to 16V, drive up to 4A (pulsed), and switches fast (14ns)[3].

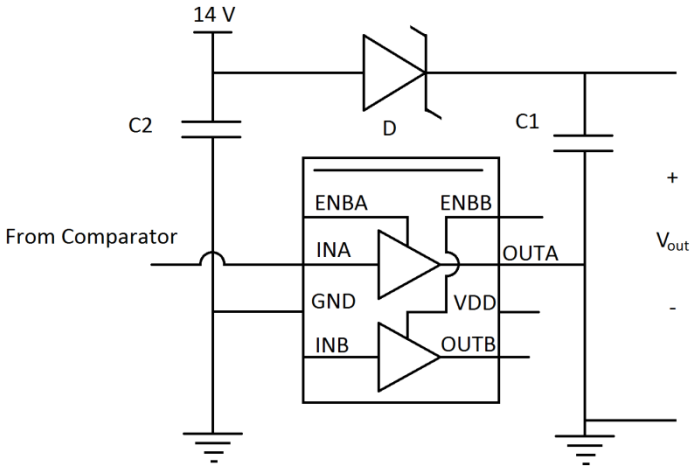

Figure 13: Voltage Doubler circuit [3].

The schotky diode (D in figure 13) forces the series connection of the 14V supply and capacitor C1 when SW1 shorts and SW2 is opens. Similar to the buffer, the diode needs to have a small forward bias voltage drop and be able to carry up to 2A of current (pulsed). The Schotky Barrier Diode NSR0320MW2T1 manufactured by On Semiconductor, is rated to be able to carry 1 amp continuous and up to 5 amps pulsed and has a forward bias voltage drop of 0.24V satisfying the design requirements[5].

Testing: Prior to integration of the three block design, testing of the doubling block under expected/harsh conditions determines the expected operation of the circuit. To emulate the heavy loading similar to that of the class-AB amplifier, load the doubler circuit with low resistance and high power handling capability.

Test procedures:

1. Apply an $8V_{pp}$, 4V DC offset, 1MHz square wave with 5% duty cycle to the buffer gate input of the doubler circuit.
2. Set V_{DD}, or the supply voltage of the doubler circuit, to 14V
3. Load output of doubler circuit with the 64.3Ω resistor with a 20W nominal power rating (or any other heavy load with high power handling capability).

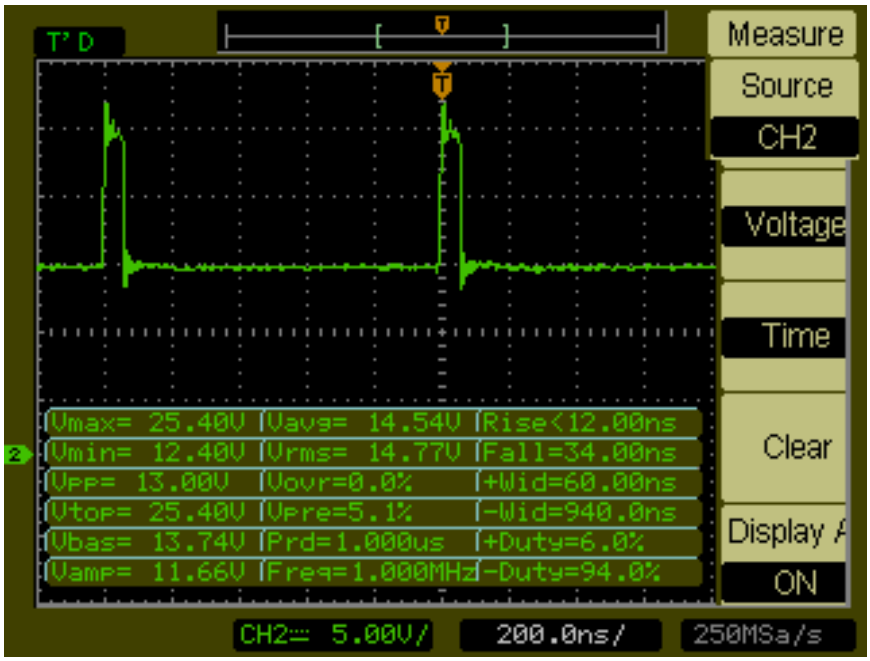

Figure 14: Oscilloscope readout at output voltage of test voltage doubler.

Figure 14 shows slightly less than ideal operation of the circuit. The output does not quite peak at 28V (due to non-ideal switching and forward bias diode voltage drop). Final design requires tweaking of supply voltage to acquire a desired peak voltage of 28V.

The average minimum voltage is sitting at 13.6V and the voltage it is getting increased to when the capacitor is discharging is at 22.2V. This is not exactly doubling but we will be able to work around this by increasing the voltage that we have our power supplied to the driver. Ringing is observed at the transitions, which could be due to long wires and large components, (the final design will have all traces on a printed circuit board). These assumptions were made because this test set up was run with banana to grabber wires to connect the load and the voltage at the output experienced considerably more ringing. Another thing to note about the voltage plot is that the doubled voltage of 22.2V is staying constant during the duration of the square pulse. If the pulse had a higher duty cycle than the time constant of capacitor C1, the discharge of the capacitor would show on the plot. The discharge would look like a ramp that would fit within the high period of the input square wave.

Complete Design

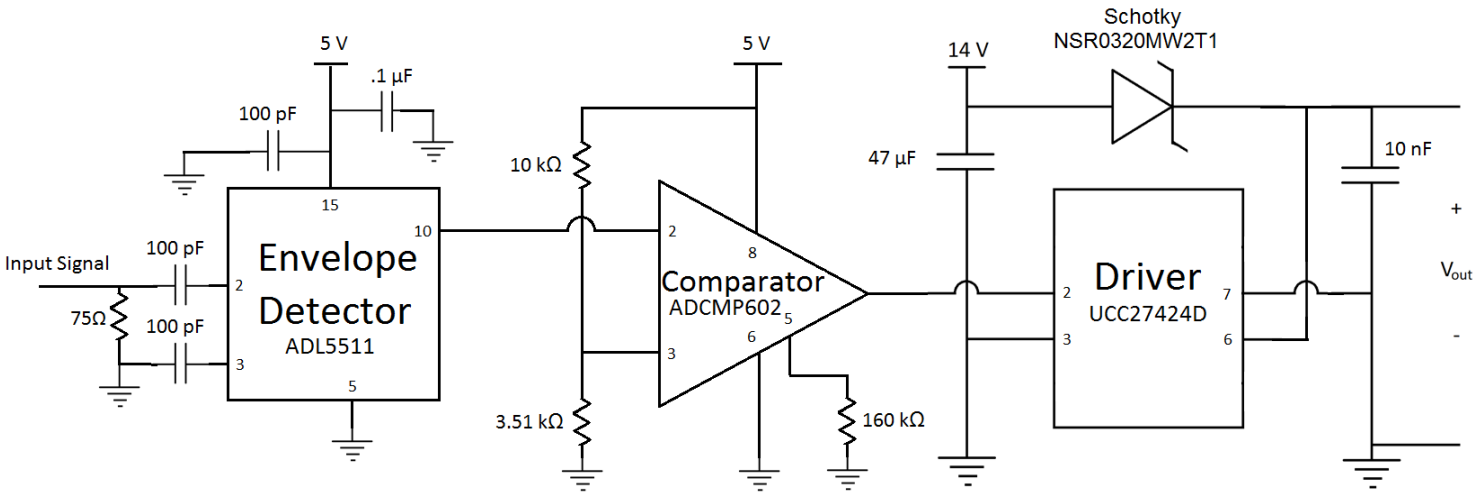

Figure 15: Circuit Diagram of Complete Design

The circuit diagram in figure 15 shows the complete design of the feed forward section of the design. The input to the Envelope Detector is the high PAR input signal and its output is a proportional voltage to the envelope of the input signal, which is then input into the comparator. The comparator outputs a high, 5V, when the input signal is above the negative input (threshold), which is set by the voltage divider. The comparator outputs low, 0V, when its input is below the threshold. The Comparator's output signal is then sent into the driver. When this input signal is low the 10nF capacitor is charging up to 14V. When the driver input is high the 10nF capacitor is discharging and the output voltage to the system is initially 28V and decays to 14V as the 10nF capacitor discharges.

TEST PLANS

In order to validate the feed-forward design, it has to be integrated with a class-AB amplifier and tested with a signal with large PAPR (>9dB). Furthermore, validation requires acquisition of a class-AB amplifier with desired performance (supply voltage, gain, P_{1dB}, frequency range, etc.) and signal generation test equipment capable of OFDM modulation with required PAPR.

After research of various high power, high frequency, transistors currently being manufactured, testing will be performed with NXP's BLF6G27-10 power transistor demo board, shown below in figure 16 [2]. This transistor provides approximately 19dB of gain, compresses at 40dBm (10W), runs off a 28V supply, and operates from 2.5-2.7GHz [2].

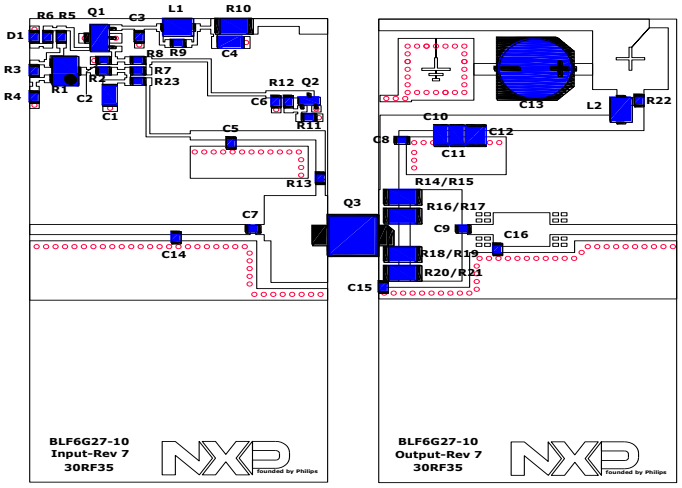

Figure 16: BLF6G27-10 Amplifier demo board layout

Given the aforementioned frequency and power range of the BLF6G27-10 power transistor, a signal generator needs to be acquired that can produce previously mentioned large PAPR signals in the 2.5-2.7GHz frequency band. After research of possible signal generator test equipment, testing will be done with two programmable boards (TSW3100 and TSW30H84), both shown in figure 17, used in conjunction and manufactured by Texas Instruments, capable of being programmed to generate LTE test

model signals (LTE signals implement OFDM) [10,11]. The basics of operation of these two boards are as follows. The TSW3100 feeds two digital streams ("in phase" and "quadrature" components) of programmed values to the TSW30H84 board at a programmable rate [10]. The TSW30H84 receives the stream of digital values, provides digital mixing (if desired), and up converts the analog signal I/Q components up to a higher frequency centered at the applied local oscillator (LO of TSW30H84). Most importantly, the TSW30H84 accepts LO frequencies in the range of 300MHz-4GHz [11].

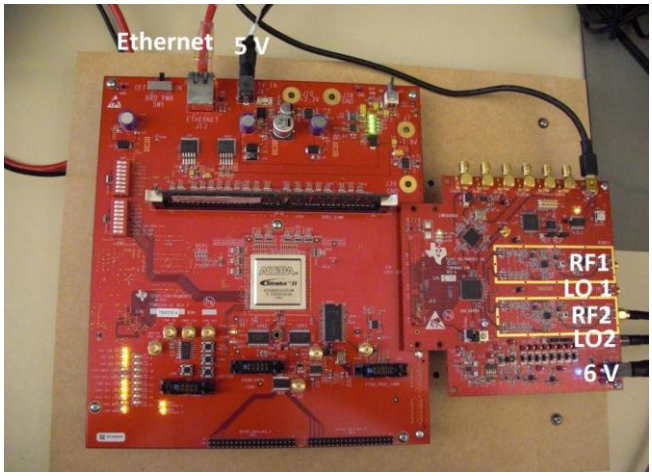

Figure 17: Signal Generator Boards

Furthermore, testing will be performed with an LTE 10MHz BW TM1 (Test Model 1) signal, as shown in Figure 18 below.

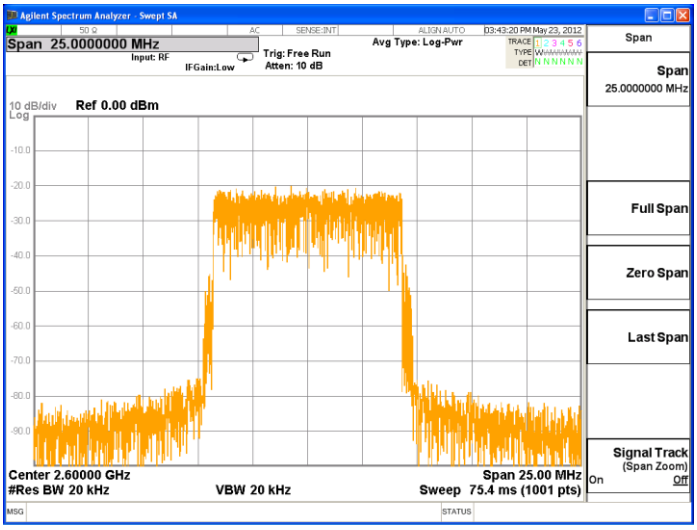

Figure 18: Frequency Spectrum of LTE 10 MHz signal

To fill out the complete test set-up, 2 gain blocks and an attenuator are required. The two gain blocks provide the sufficient gain to bring up the power of the signal output from the TSW30H84 to a level sufficient to drive the BLF6G27-10 right up to its compression point (approximately 40dBm/10W)[2]. Specifically, the ZX60-5916M+ (17dB) [6] and ZRL-3500 (18dB) [7], in conjunction, provide 35dB gain while not compressing and will be used for testing. Although an excessive amount of gain, this will allow for the output of the TSW30H84 to be backed-off (on-board digitally adjustable attenuator). In order to be able to measure the output spectrum of the complete class-G power amplifier, the signal power must be attenuated below upper power limit of the Agilent CXA spectrum analyzer, 30dBm. Sufficient attenuation of the amplifier out is realized by use of the (part) 30dB attenuator, as shown in figure 19.

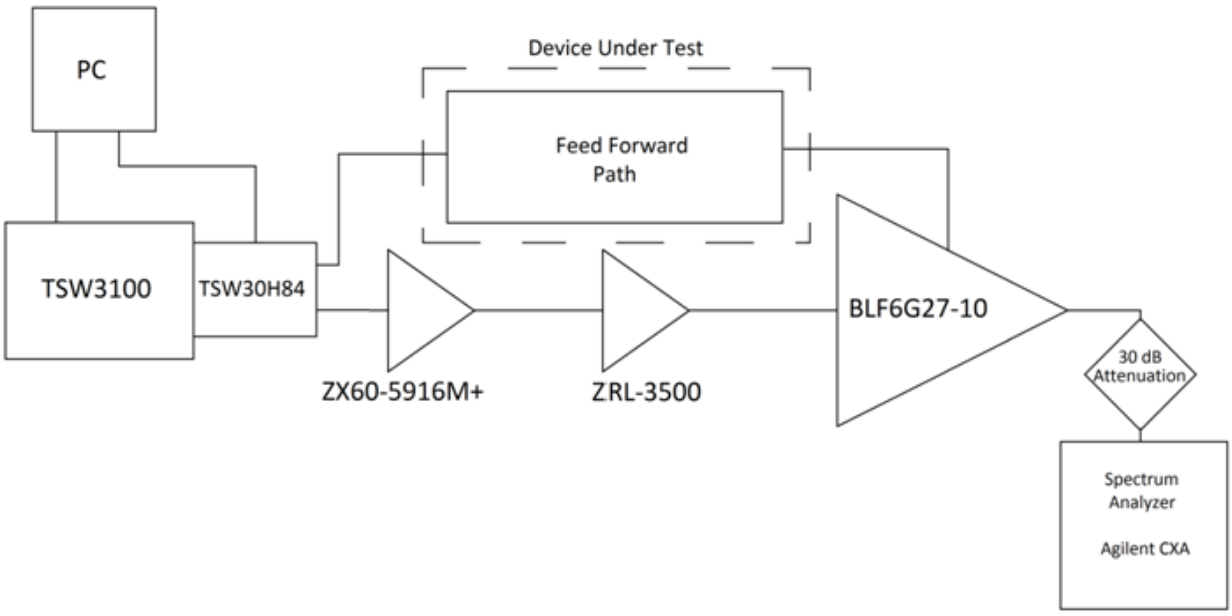

Figure 19: Flow Diagram of test setup

INTEGRATION AND TEST RESULTS

The next step in testing the design is to put all three components together and use the high PAR signal discussed above. The signal used for this test was the 10MHz LTE test signal. Its PAR is around 10 and was set to a center frequency of 2.6GHz, to more closely follow final design testing. The signal was first put through the envelope detector, then through the comparator and finally through the voltage doubler. Before testing according to the test plans above, the DUT was loaded with a 53Ω and a 45Ω resistor in series, each with a 20W power rating, to exemplify the heavy loading (large current draw) of the NXP amplifier.

The output of the envelope detector was probed on an oscilloscope, and a signal similar to the one tested in the envelope detector section was found, figure 20. The highest peak was around 2.25V and the average voltage was around 1.3V. The peak voltage was higher than the previously one tested because this was the 10MHz LTE signal, which has a higher PAR, so a higher peak value is expected.

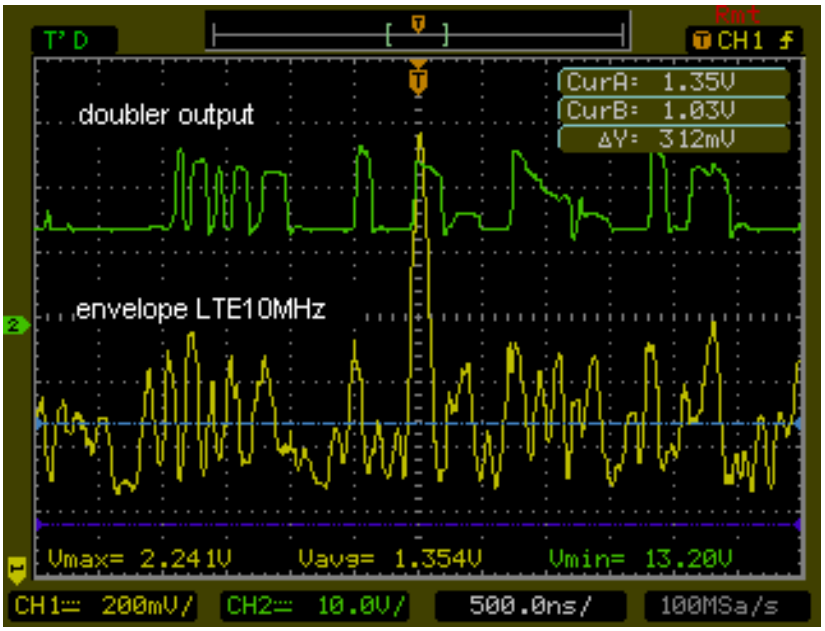

Figure 20: Envelope detector and Voltage Doubler Output

The output of the envelope detector can be seen below in figure 20(the yellow signal) and the comparator output was probed to check for proper functionality, and was found to jump from 0V to 5V according to the envelope detector. The output of the voltage doubler was then tested to see if the voltage doubled from 14 to 28V when the envelope detector surpassed the comparator threshold. As seen with the green signal in figure 20, the doubler jumped from 14 to 28V when there was a spike in the envelope detector.

To further load the designed circuit the 64Ω load was removed, leaving the circuit only loaded with a 53 Ω resistor. This will strain the circuit more because it will try and draw more current from the doubler.

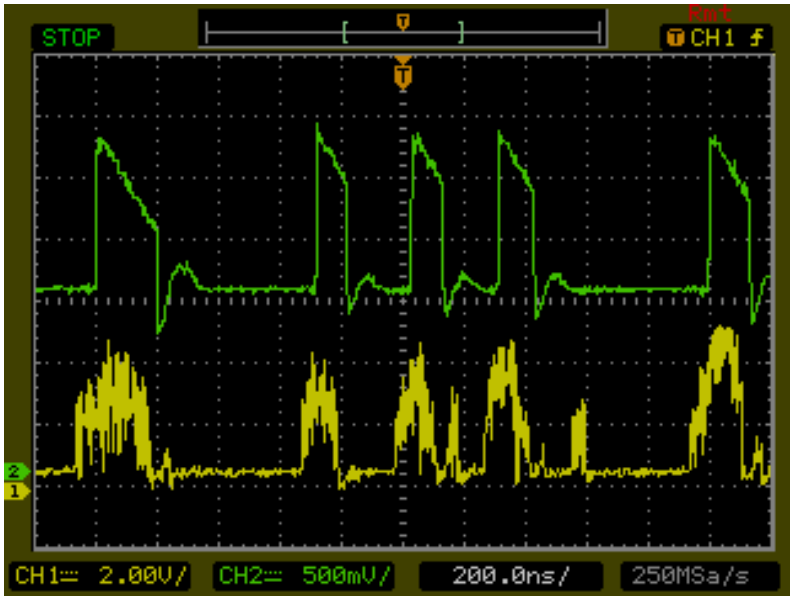

Figure 21: Comparator and Doubled output

Shown in figure 21 are the comparator output (yellow) and the doubled output (green). The comparator output appears noisy, which could be due to the envelope carrying noise from the original (high PAR) signal, but its functionality remains intact. The doubled voltage should be activated when the comparator output is high. For this test, the peak power output from the signal generator board was set 6dB above -2.5dBm. The -2.5dBm value came from the test of the envelope detector, and was the input

power required for the envelope output to have an average output voltage at 1.33V. The signal generator board was set to 4.5dBm because the peak power value is ideally located at twice the comparator threshold voltage. An increase of 6dBm is equivalent to a multiplication of 2 to its voltage. The doubled voltage (the green signal in figure 22) was observed to "double" from 13 to 25V. Since, 28V are required for the NXP amplifier, the supply voltage of the driver was increased from 14V to 15V. This slight change was able to accommodate, and increased the output voltage range to its required range. It now doubles from 15 V to 28V.

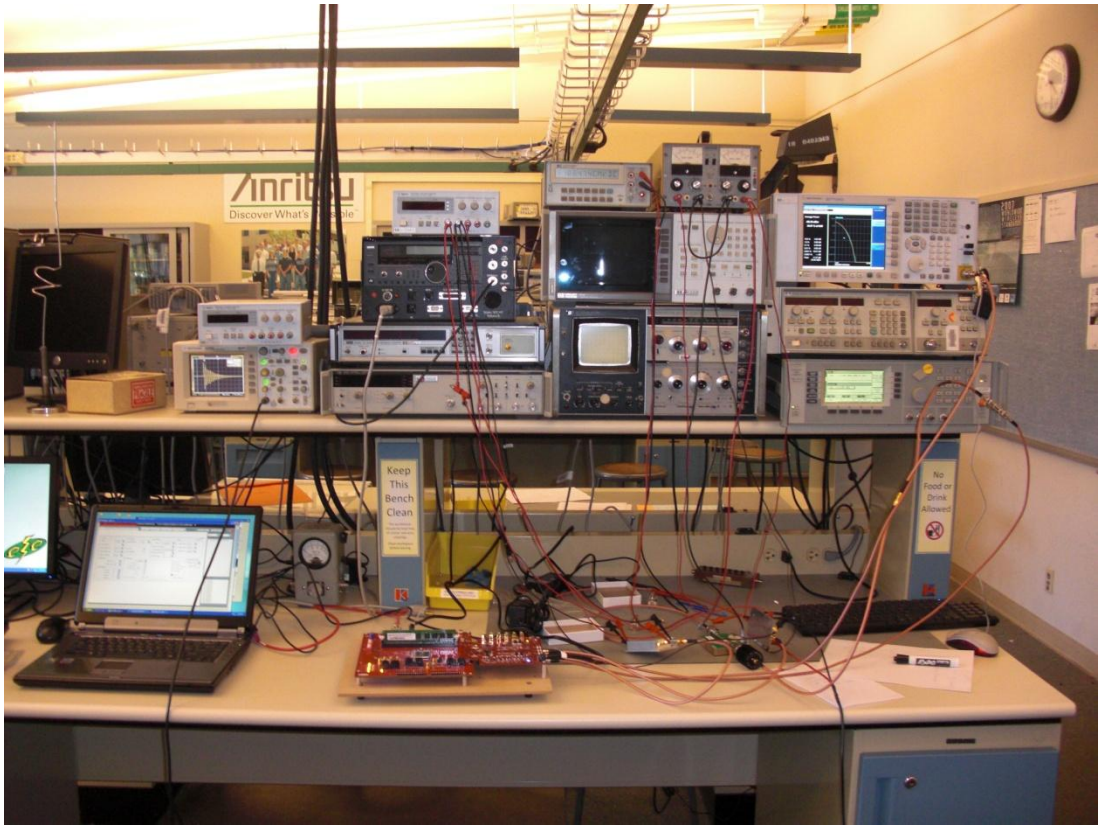

Figure 22: Lab test setup for amplifier integration testing

The lab setup pictured in figure 22 is a physical representation of the flow diagram in figure 19. The BLF6G27-10 amplifier was used to load the designed circuit. This amplifier requires a higher input power than the signal generator board can output so the two preamps were applied between the amplifier and the signal generator board. The spectrum of the signal after the two preamps is shown in figure 24. It is important for this spectrum to be similar to the signal generator because, any distortion

added to the spectrum should come from the BLF6G27-10 amplifier, as a control to the test setup. This spectrum, shown in figure 23, has some added distortion (spectral re-growth) from the two preamps which required the output of the TI signal generator to be backed-off using the on board variable digital attenuator.

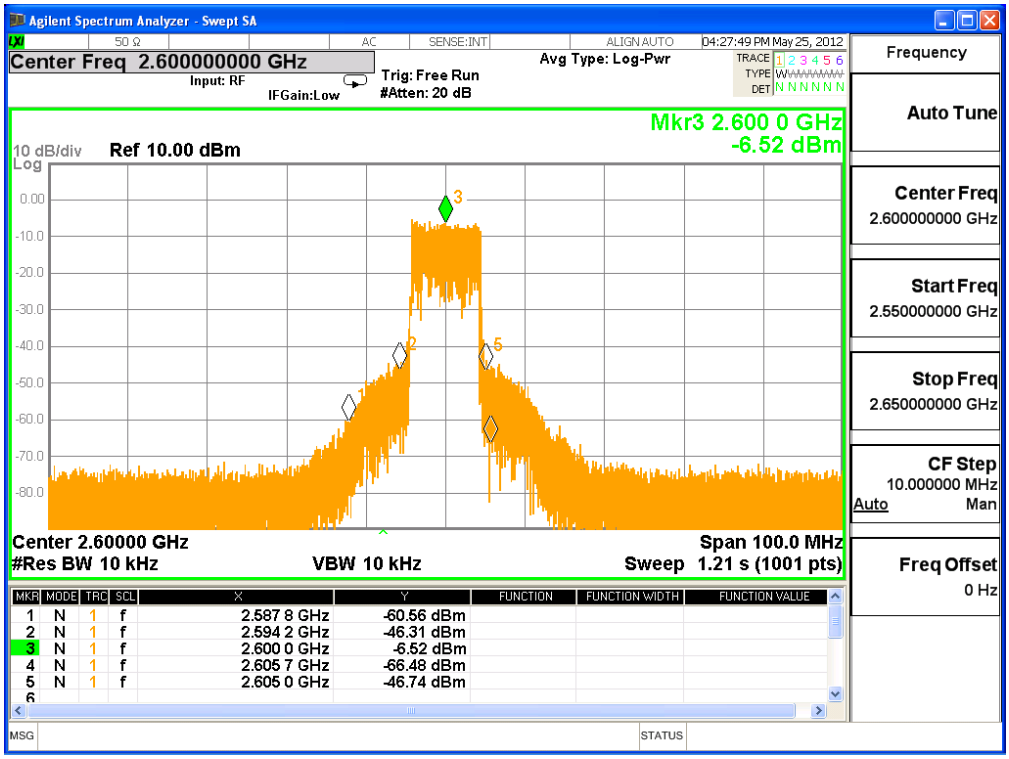

Figure 23: Frequency Spectrum of signal, after two preamps (prior to the BLF6G27-10 amplifier)

To test the performance of the designed circuit, three spectra will be compared. First the best case scenario will be tested by supplying a constant 28V to the drain of the BLF6G27-10 amplifier. Then the worst case scenario will be tested by supplying a constant 14V to the drain of the BLF6G27-10 amplifier. Finally the design will be tested, which provides either 14 V or 28V depending on the input signal instantaneous power. What is expected is the 28V supply will have the least amount of out of band distortion, the 14V supply will have the most out of band distortion, and the supply modulation technique employed by the designed circuit will be somewhere in between .

The spectrum when applying a constant 28V, came out as expected, with very little skirting. Then the 14V supply was tested and some skirting occurred, although less than expected, and can be seen in figure 24. Also in figure 24 is the frequency spectrum of the signal when the supply modulation technique is applied.

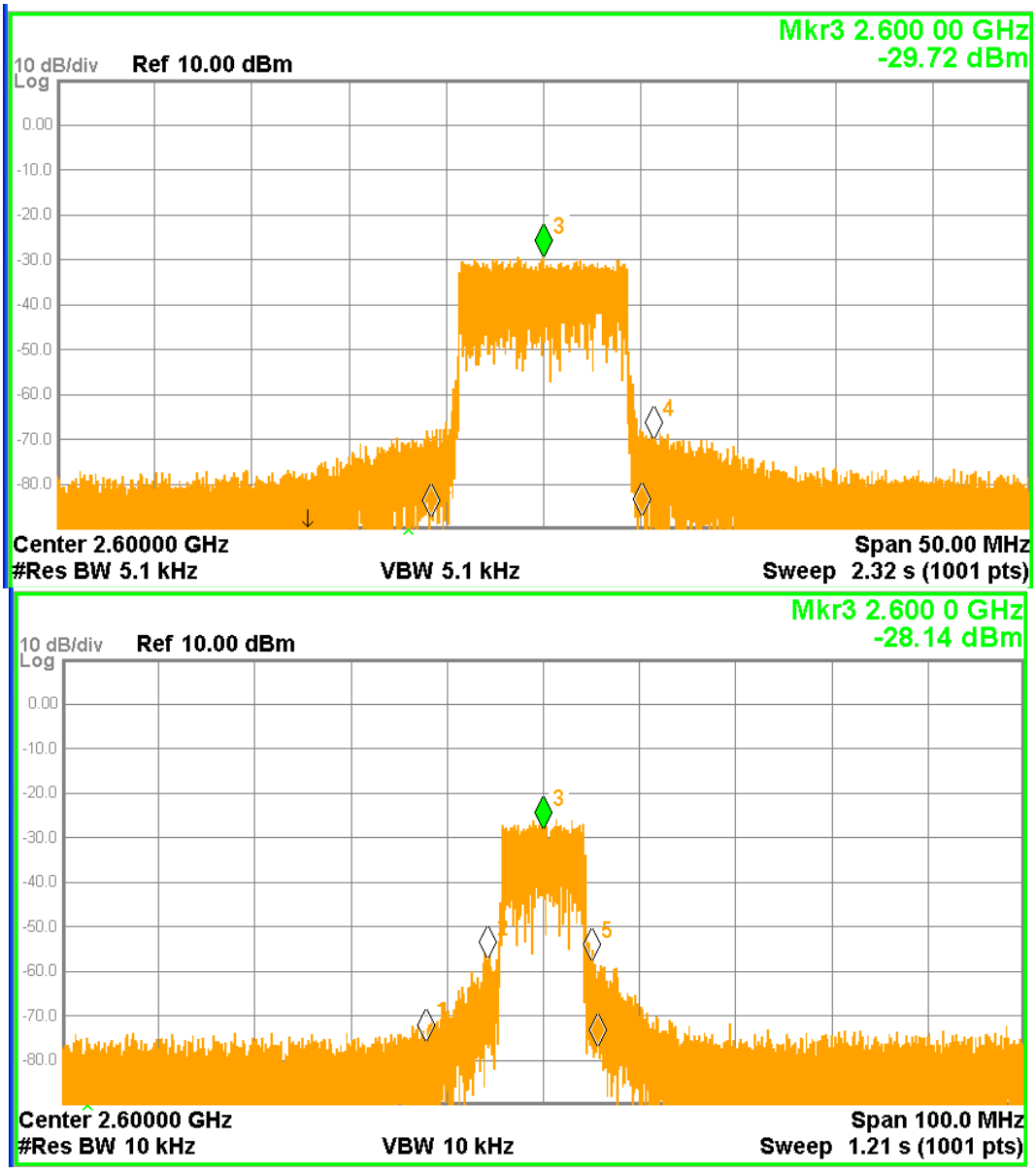

Figure 24: a) Frequency Spectrum with 14V supply b) with modulation of supply

It can be seen that the design added more distortion to the signal than was observed at half supply, as more skirting occurred with it than operation with a constant 14V drain supply.

Upon further examination of the voltage doubling module (DUT) output when being tested with the NXP amplifier evaluation board, unexpected performance occurred (shown in figure 25 below).

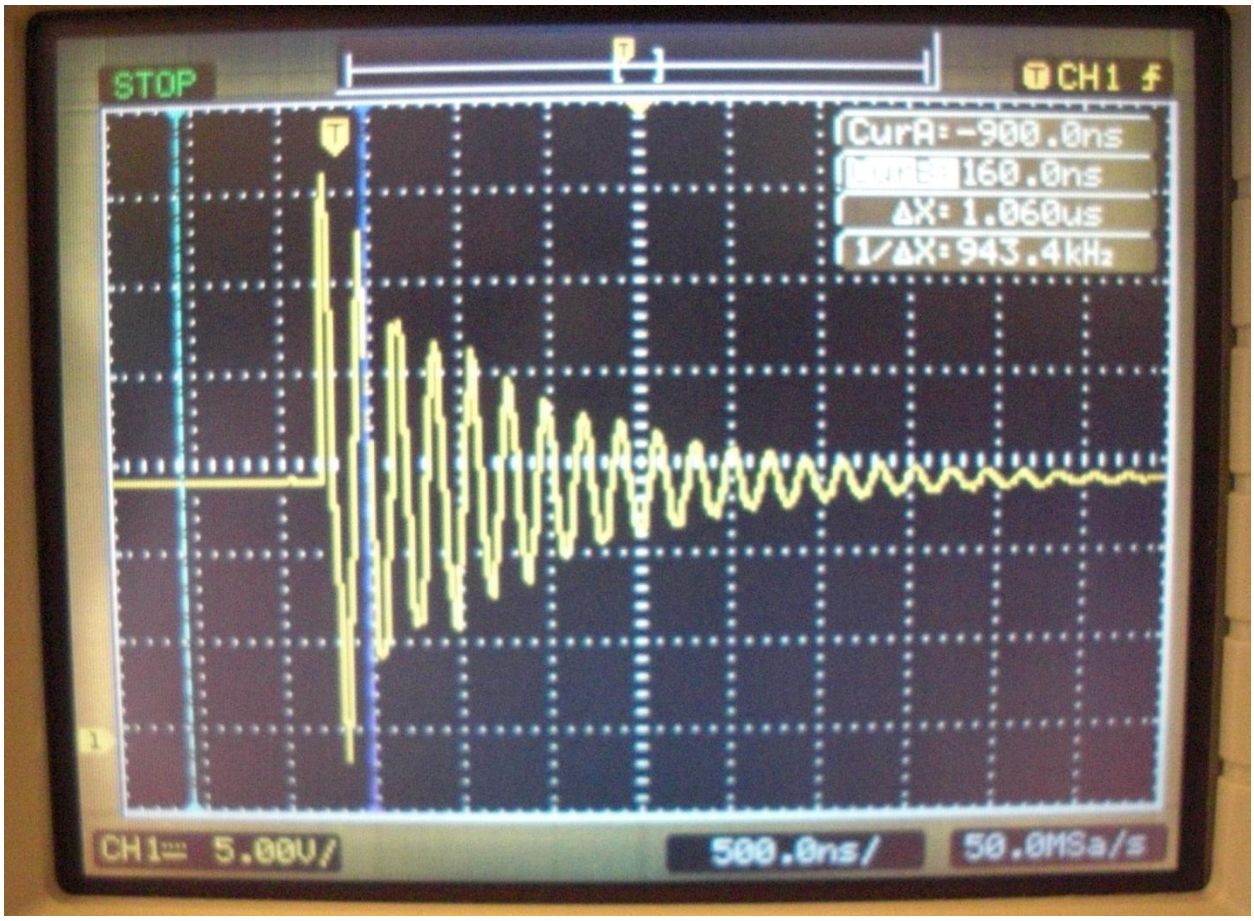

Figure 25: Output of DUT under test plan conditions

Figure 25 resembles an under-damped ringing response, which peaks at a voltage greater than 30V, but rings to a steady state voltage of 15V. Ideally the output of the DUT would be the envelope of this signal, but the results suggest the decoupling reactances of the amplifier evaluation board are causing the under-damped step response. The DC supply decoupling circuit of the amplifier board looks like the schematic shown the Figure 26 below.

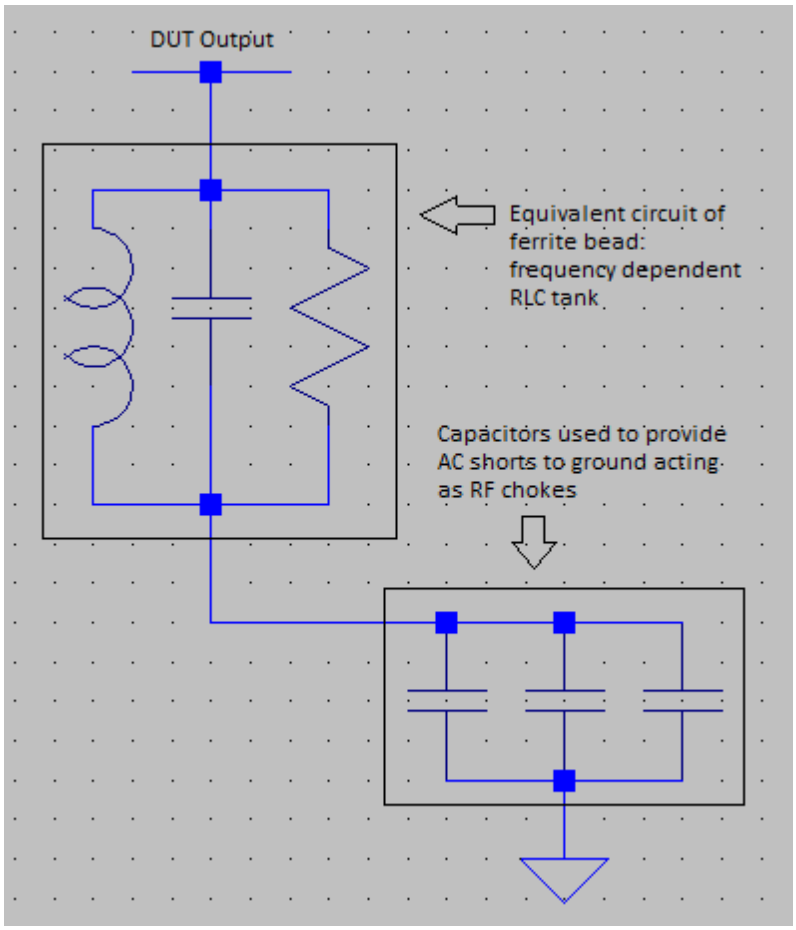

Figure 26: Equivalent circuit at DC supply node of NXP amplifier

At the frequency of operation, the resistance and capacitance of the ferrite bead can be ignored and the total capacitance of the AC shorts to ground can be modeled as the dominant (10µF from datasheet) capacitor. The inductance of the ferrite bead at the frequency of operation can be determined from the datasheet reactance graphs, shown below, and at 10MHz the bead looks approximately like a 250nH inductor:

$$L = \frac{15\Omega}{2\pi(10^7)} = 250nH$$

Now that the component values of the equivalent circuit have been determined, a step response simulation can be run to determine an accurate representation of the observed ringing during testing. Figure 28 shows the circuit used for simulation.

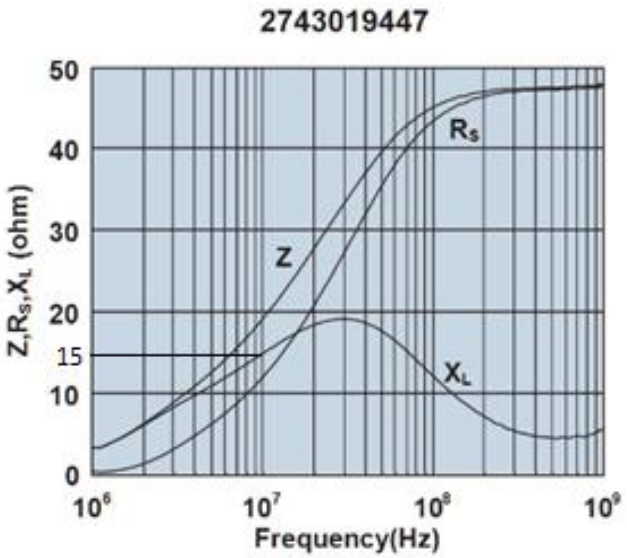

Figure 27: Reactance vs. Frequency of Ferrite Bead. [8]

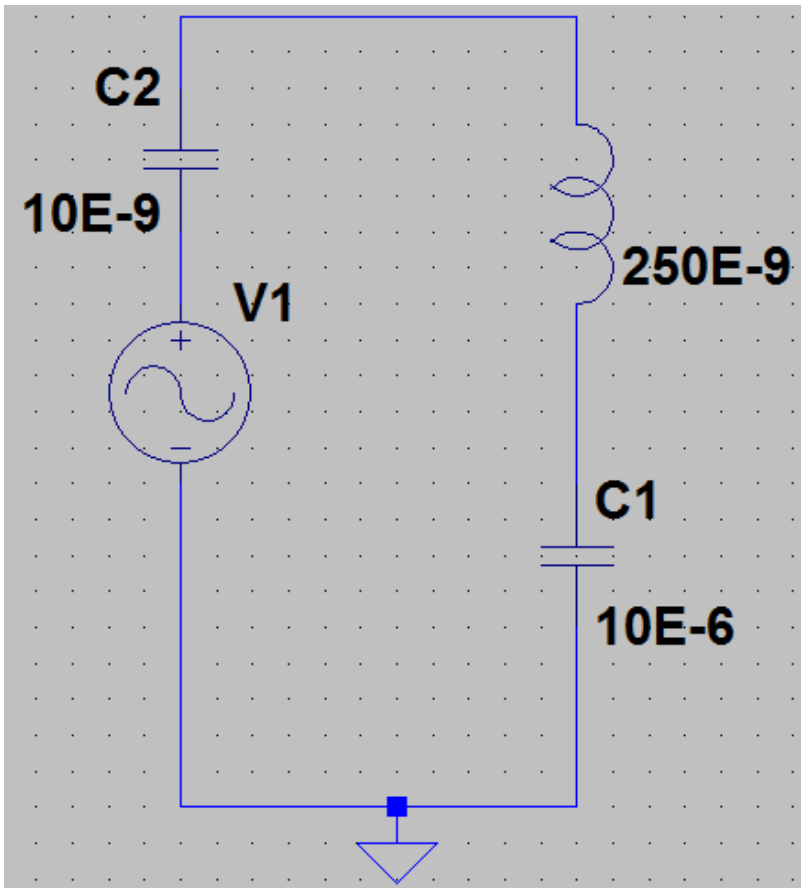

Figure 28: Circuit used for simulation to verify ringing results

The simulation results of this circuit show a resonance occurring at a frequency of approximately 3-4MHz (Figure 29) and swings 28V_{pp}, which is in the ballpark of the 5MHz and 30V_{pp} ringing observed during testing. Given these results/findings, the voltage doubling design needs to be modified to account for the DC coupling and RF choking of the ferrite bead used on the NXP amplifier board.

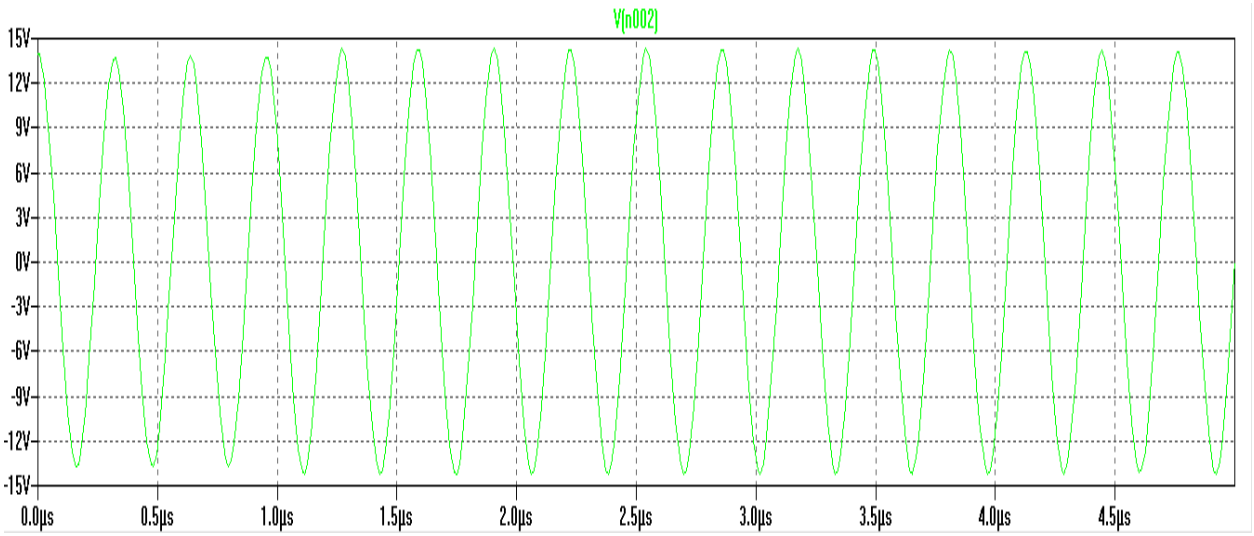

Figure 29: Simulation results: displaying voltage at equivalent DC supply node

CONCLUSION

Although we were not able to integrate our design with the class G amplifier, testing with a dominantly resistive load proved correct functionality. The design failed to interact with reactive load components present on the BLF6G10-135RN power LDMOS transistor evaluation board. The design still maintains its possible validity because it was able to drive a powerful load (50Ω), proving fast and powerful voltage spikes, to account for a peak in a high PAR signal, are obtainable. The supply voltage spikes were able to carry a large enough current to power a transistor. The next step in testing this idea is to create a design that takes into consideration the reactive components on the power amplifier evaluation board.

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APPENDICES

Appendix A: Senior Project Analysis

ABET Senior Project Analysis

Project Title: Wireless Base Station Power Amplifier

Student's Name: Kevin Maulhardt, Kevin Haskett

Student's Signatures:

Advisor's Name: Vladimir Prodanov

Advisor's Signature:

Date:

1. Summary of Functional Requirements

   The design takes two inputs, DC power and RF signal, and outputs a efficient, linear, and amplified RF signal of the RF input. The output signal of the design drives a 50 ohm load (antenna) which requires suffienct power (of the RF signal) to propagate the signal through the air a sufficient distance.

2. Primary Constraints

   The design's must comply with the following primary contraints: 3GPP linearity regulations; high power efficiency; sufficient output power; sustainable, robust operation; ability to test and verify operation.

3. Economic

The design project has the following economic impacts: design/build/test time spent; labor pertaining to ordering/shipment of parts; estimated cost of parts ($220); cost of labor ($10,260); costs of test equipment and manufacturing equipment ($920); use of earth's materials used in the parts used (silicon, copper, dielectrics, structual materials); funding for project costs;

Costs of the project accrue from time spent on design/build/test, purchase of parts from component manufacturer's, purchase/availibilty of test equipment. The costs of parts and test equipment result from the design parts and test equipment and the material required to make the parts and equipment. The material for the parts and test equipments require earth's natural materials to be processed and manufactured to create their products. The costs of the design are outlined in the cost estimates table, Table 2.

The project potentially produces a design that can be manufactured and implemented in wireless communication systems. The project earns the designers technical and project experience appplicable to the RF engineering discipline. Designers and companies whose products are used in the design profit from the project. Companies invested include parts manufacturers, transportation companies, Cal Poly university employees, etc because their services are required to produce the final product.

Products of the design project emerge at the end of Spring quarter 2012 and are evaluated for manufactuability. Outline of project timeline and milestones are included in Gantt chart form in figures 3 and 4.

Appendix B: Schedule

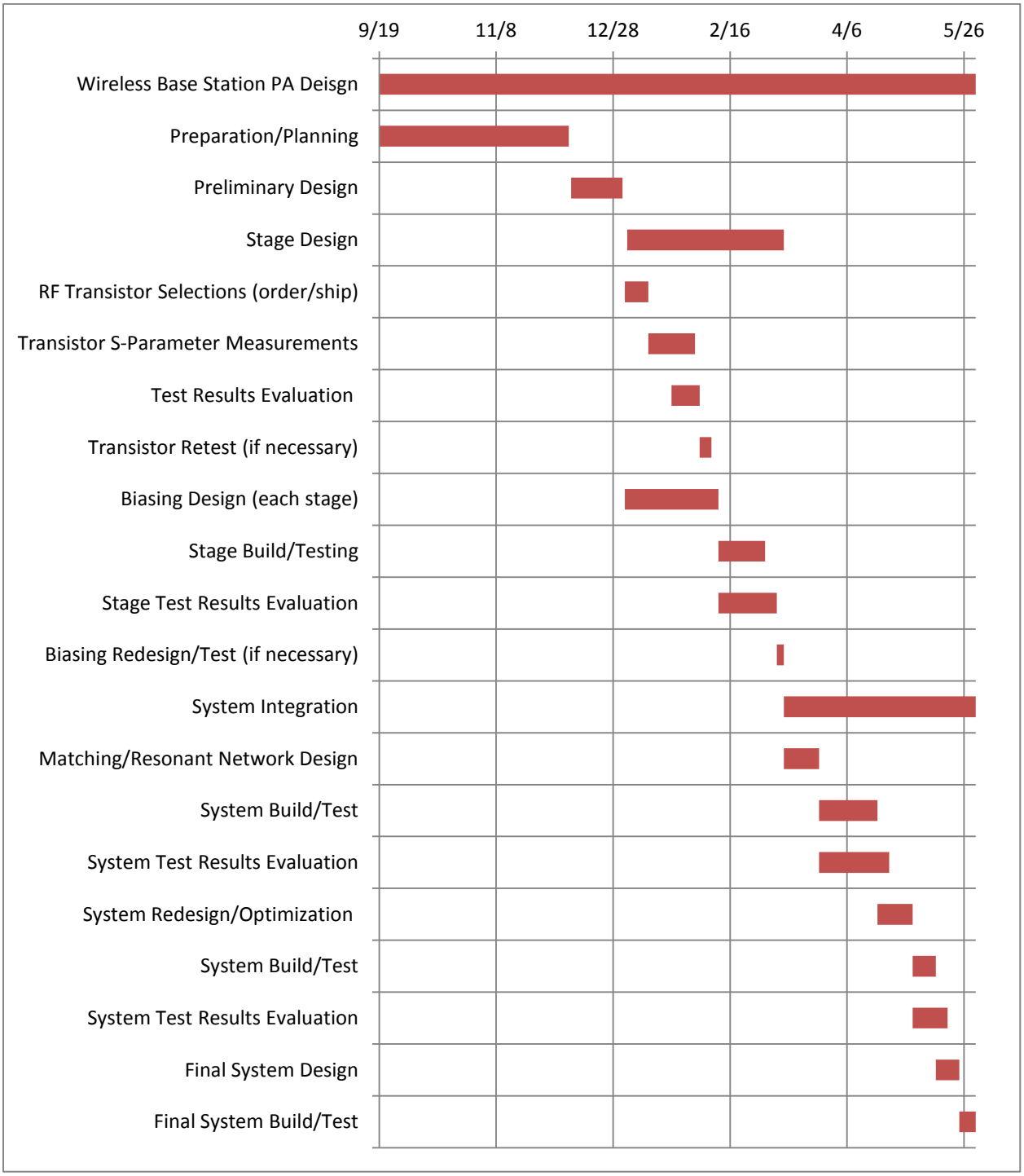

Figure 30: Wireless base station power amplifier design Gantt chart

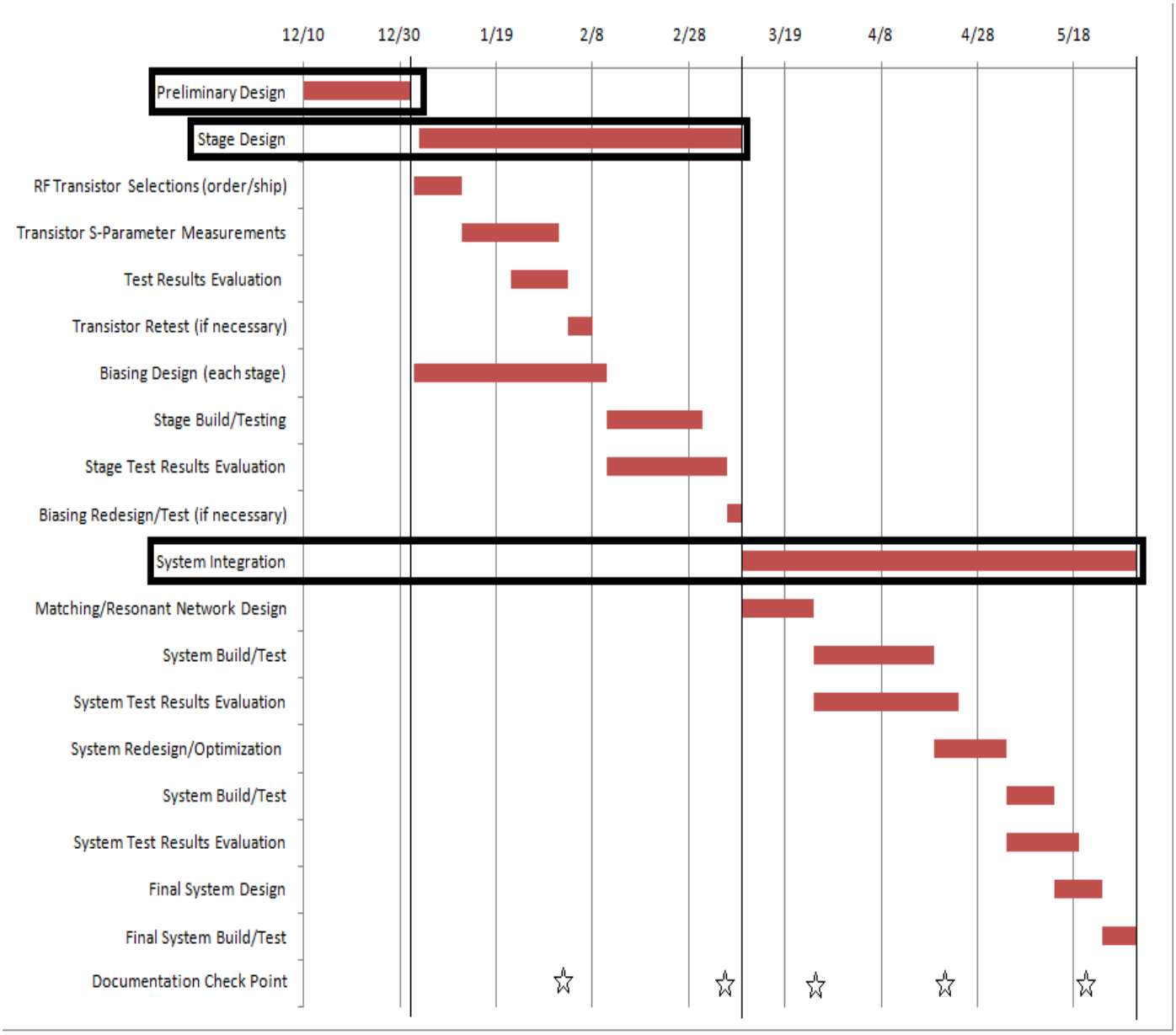

Figure 31: wireless base station power amplifier design Gantt chart

APPENDIX C: Cost and Production Analysis

Table III.

DESIGN AND COST ESTIMATES

Cost Type	**Cost Esitmate**
Labor – time spent preparing, designing, building, and testing	[(250) + 4(350) + (400)] / 6 = 342 hours (342 h)(30 $/h) = $10,260
Parts/Build – cost of any components used in design, as well as board fabrication materials/machining	[(175) + 4(200) + (350)] / 6 = $220
Test Equipment – cost of EVMs, use of lab equipment and facilities, any extra lab equipment needed to be purchased.	[(500) + 4(750) + (2000)] / 6 = $920

1. If manufactured on a commerical basis:

   The project consists of verifying a design concept for class-G RF power amplifier design. If the concept succeeds, manufacturing on a commerical basis could take place indirectly through industry.

   Estimated number of devices sold per year: 2 million (potential to be used in any wireless device)

   Estimated manufacturing cost per device: $10

   Estimated purchase price per device: $15

   Estimated profit per year: $10 million

   Estimated cost for user to operate device (specify time interval): 240 Wattxhours

2. Environmental

   The project requires natural resources to be consumed in order to produce a final operating product. Natural resources include fossil fuels, silicon, copper, dielectrics, etc. Fossil fuels are required to operate transportation vehicles used to ship parts, power test euipment and project modules, extract materials used in product, and operate fabrication machinery. The project aims to reduce the amount of energy needed to power a wireless transmitter, therefore reducing the consumption of natural energy resources used in current wireless transmission system. The energy required to produce and power the project final product requires the external environment to be polluted harming humans and all species that inhabit the earth.

3. Manufacturability

   The size and low tolerance of parts are issues related to manufacturability of the final product of the design project. Slight inaccuracies of connectors will cause wave reflections that can damage the module.

4. Sustainability

   The device must operate at high output power which requires that the parts compliance while still maintaining precise operation over very long periods of time. Natural resources are used to power the device, machines used to manufacture the device, test equipment, and transportation vechicles used to transport parts and materials. The design can be upgraded to be more power efficient and less delicate to part tolerances. In order to upgrade the design, new power amplifier design techniques must be improved through research.

5. Ethical

   Based on the ethical framework treat others the way you would like them to treat you, the following are ethical issues involved with the project design: security of transmitted data; harmful effects of electromagnetic radiation on living things; ecosystems harmed by the production of the device. In order for the power amplifier to be eithically accepted, the information being transmitted wirelessly must be secure. Third parties must not be allowed to gain access to the communication of the primary parties (IEEE COE Code 2). Also, if the device is to malfunction or operate defectively, precaution must be taken to make sure that the electromagnetic radiation of the system does not cause harm to anything living (IEEE COE Codes 1 and 9). Throughout the entire design/ build/manufacture process, emissions from fossil fuels burned in order to power the device and machines used to extract the necessary materials and manufacture parts can harm ecosystems (IEEE COE Code 9).

6. Health and Safety

The manufacture and operation of the designed product requires fossil fuels to be burned. Burning of fossile fuels depletes a natural resource that is non-newable and emits pollutants that are harmful to humans and living species. Additionaly, the burning of fuels disturbs the equilibium of the environment that species live in and requires those living in the environment to adapt.

7. Social and Political

The efficiency of power amplification impacts the cost of wireless communication. Cheaper costs of wireless communication reduces the cost to society to use applications of wireless communication (internet, cellular devices, etc). Increased use of wireless devices has skyrocketed in the recent past and continues today. Companies who produce front-end, analog communication modules, as well as producers of digital devices that feature wireless comunications are direct stakeholders in the design project. The economic success of the communication devices directly pays the salaries of the employees of the companies who produce the devices. Individuals who use devices that feature wireless communication are indirect stakeholders in the project. Cheaper, more efficient, and better quality wireless communication systems benefit nearly every person who uses the communication devices. The direct stakeholders profit more than the indirect stakeholders because the user pay them to use their product. Any product that leads industry draws indirect stakeholders in politics because political leaders will seek to improve the success of the product in order to fund their campaigns.

8. Development

The design project requires background information on power amplification techniques (types of PAs) and techniques to go about linearizing and increasing efficiency of PAs. The project also requires research on the the current status of RF power amplification and the current issues facing designers of RF amplification devices.

Appendix D: Printed Circuit Board Layout

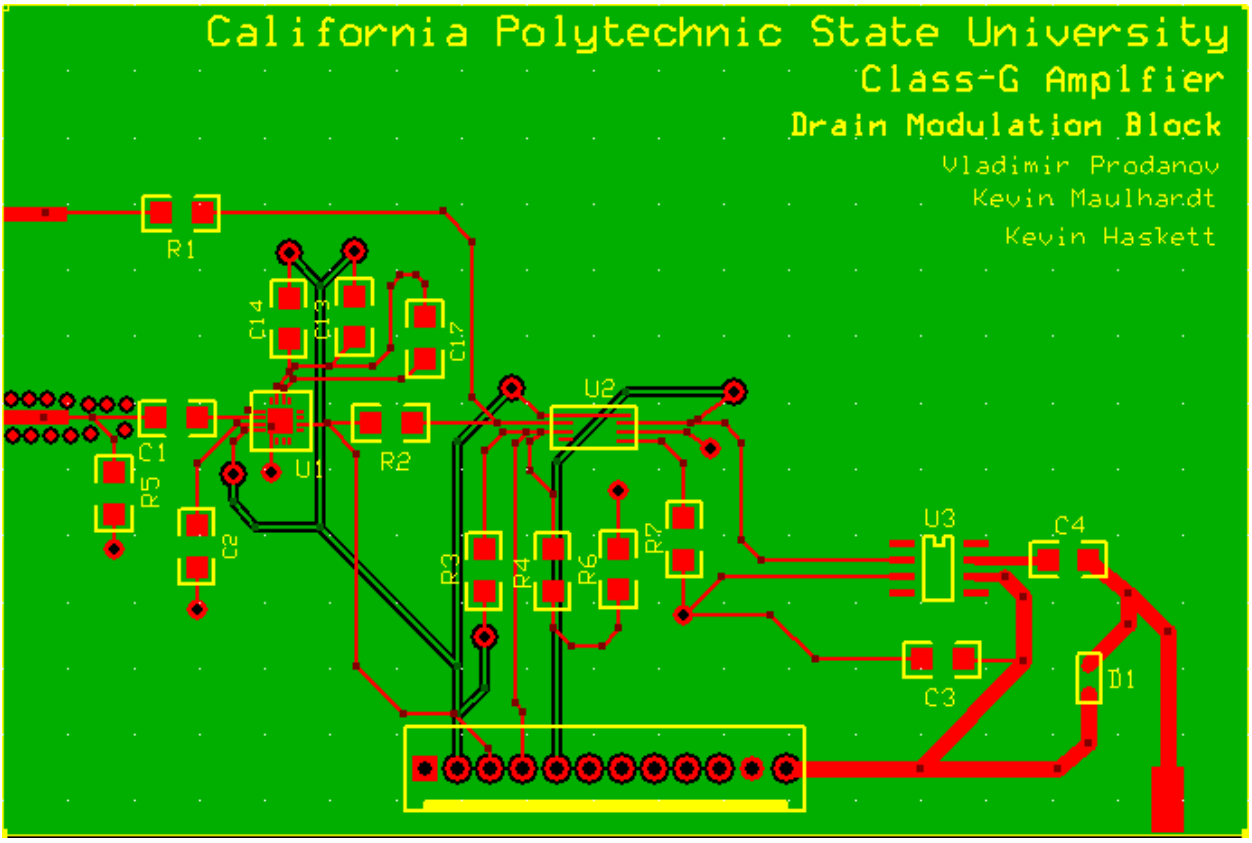

Figure 32: Printed Circuit Board Layout for design

Appendix E: Recorded Test Data

Table IV

RECORDED ENVELOPE DETECTOR TEST DATA

Pin (dbm)	Venv (V)		Pin(dbm)	Venv (V)
-10	1.222		2	1.455
-9	1.232		3	1.493
-8	1.244		4	1.535
-7	1.256		5	1.583
-6	1.27		6	1.636
-5	1.285		7	1.697
-4	1.303		8	1.763
-3	1.321		9	1.841
-2	1.343		10	1.925
-1	1.366		11	2.02
0	1.392		12	2.128
1	1.422		13	2.254